

# **EXHIBIT M**



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Tomita et al.

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(45) **Date of Patent:** Sep. 18, 2001

(54) **SEMICONDUCTOR DEVICE RECONCILING  
DIFFERENT TIMING SIGNALS**

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both of Kawasaki (JP)

(73) **Assignee:** Fujitsu Limited, Kanagawa (JP)

(\*) **Notice:** Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
U.S.C. 154(b) by 0 days.

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(22) **Filed:** Jan. 29, 1999

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(51) **Int. Cl.** ..... **G11C 8/00**

(52) **U.S. Cl.** ..... 365/233; 365/230.08; 365/189.05

(58) **Field of Search** ..... 365/233, 230.08,  
365/189.05, 240

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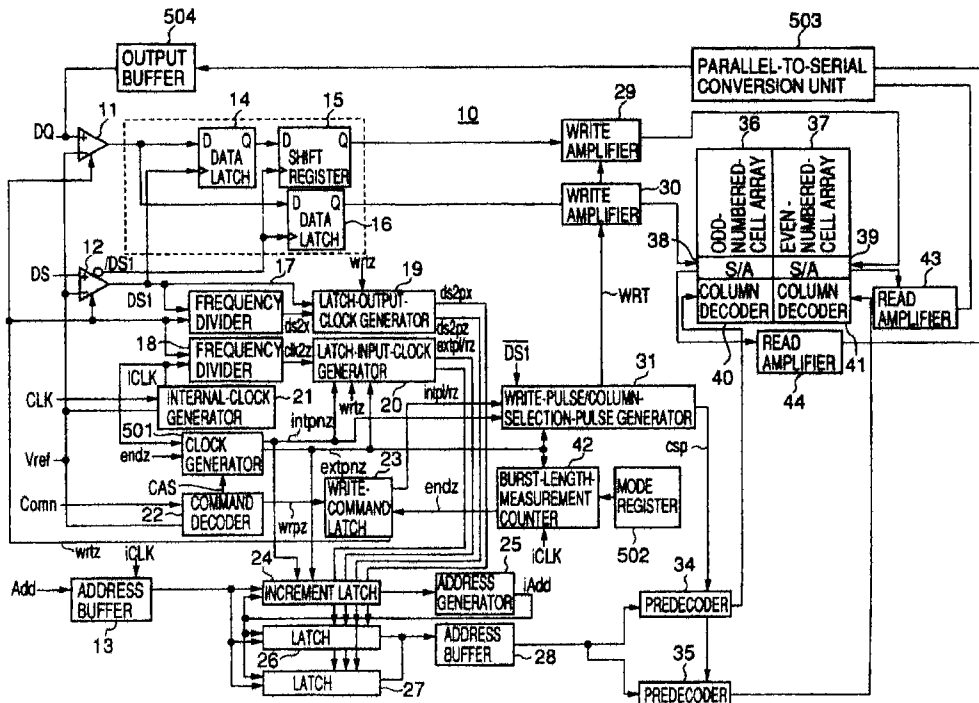
*Primary Examiner*—Huan Hoang

(74) *Attorney, Agent, or Firm*—Arent Fox Kintner Plotkin  
& Kahn, PLLC

#### (57) **ABSTRACT**

A semiconductor device which receives addresses in syn-  
chronism with a clock signal and receives data in synchro-  
nism with a strobe signal includes address-latch circuits, a  
first control circuit which selects one of the address-latch  
circuits in sequence in response to the clock signal, and  
controls the selected one of the address-latch circuits to latch  
a corresponding one of the addresses in response to the clock  
signal, and a second control circuit which selects one of the  
address-latch circuits in sequence in response to the strobe  
signal, and controls the selected one of the address-latch  
circuits to output a corresponding one of the addresses in  
response to the strobe signal.

42 Claims, 25 Drawing Sheets



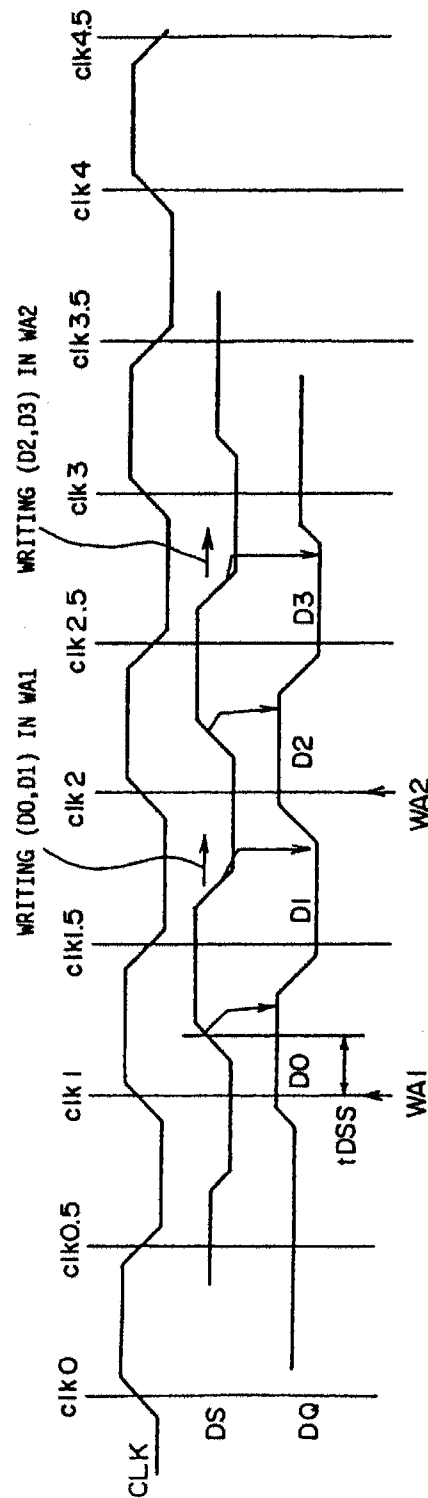
U.S. Patent

Sep. 18, 2001

Sheet 1 of 25

US 6,292,428 B1

FIG. 1



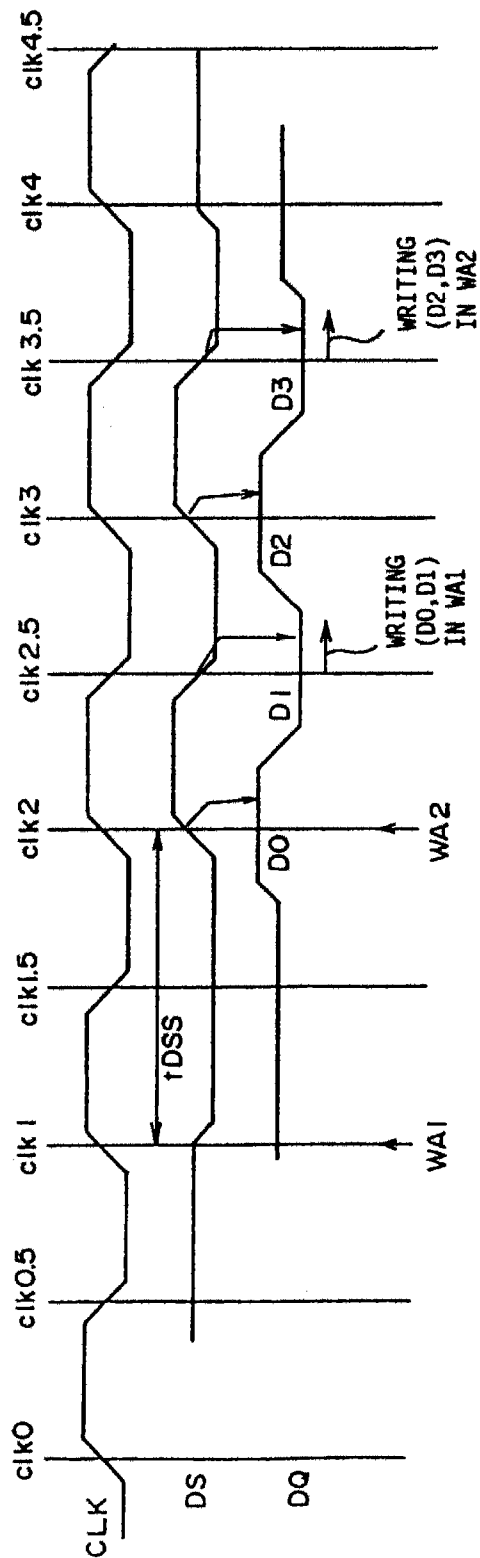
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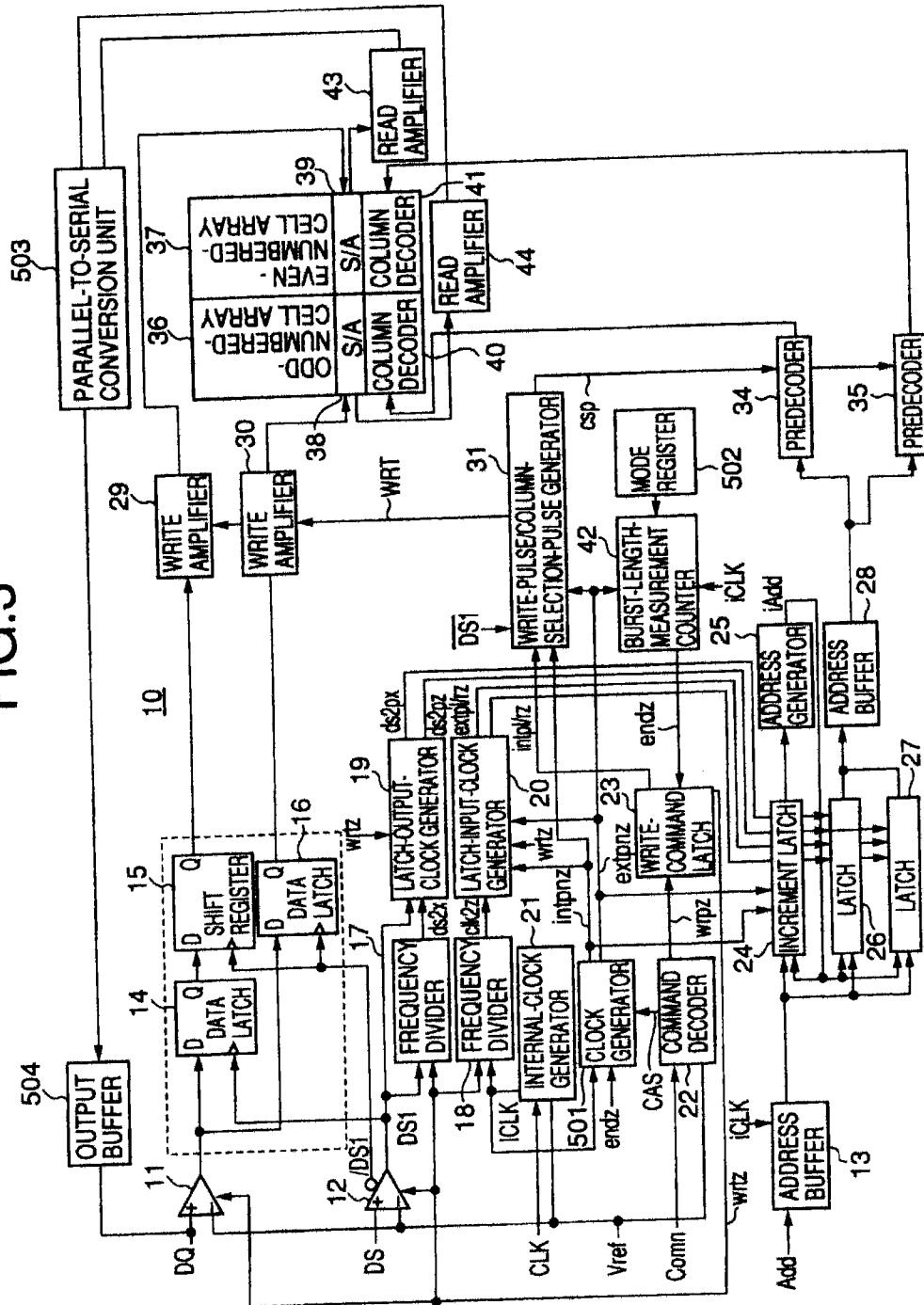
Sheet 2 of 25

US 6,292,428 B1

FIG. 2



**FIG. 3**

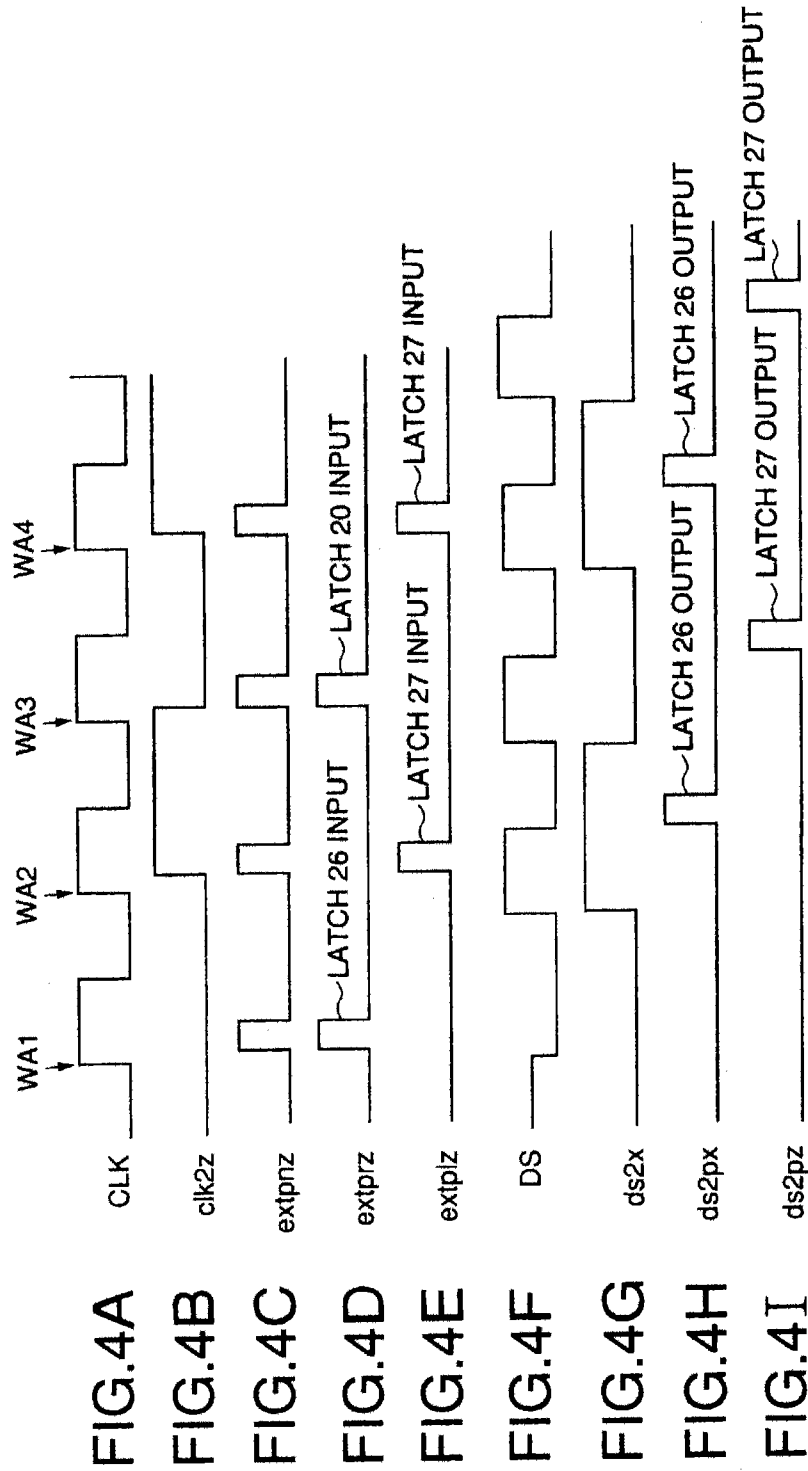


U.S. Patent

Sep. 18, 2001

Sheet 4 of 25

US 6,292,428 B1



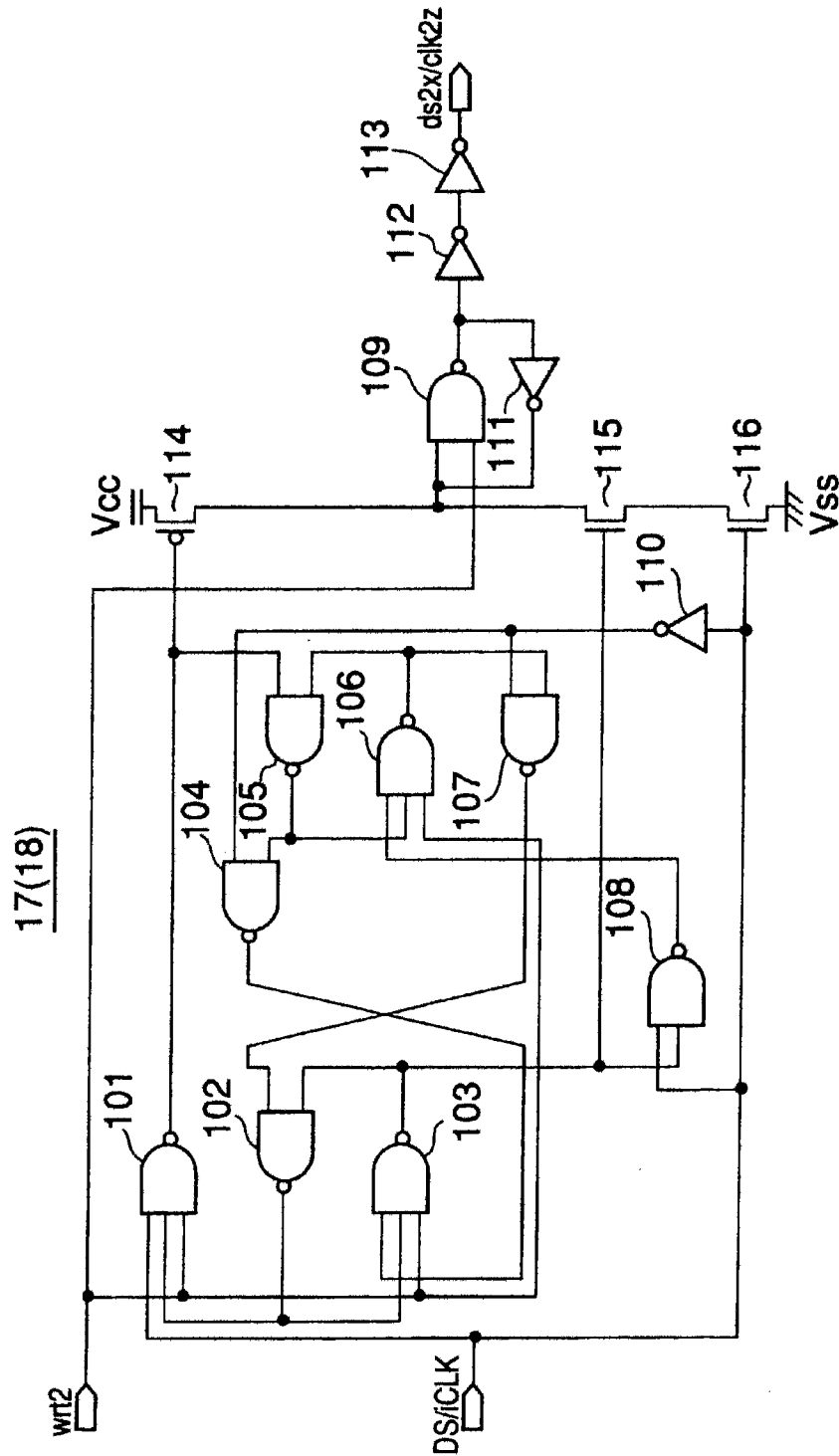
U.S. Patent

Sep. 18, 2001

Sheet 5 of 25

US 6,292,428 B1

FIG. 5



U.S. Patent

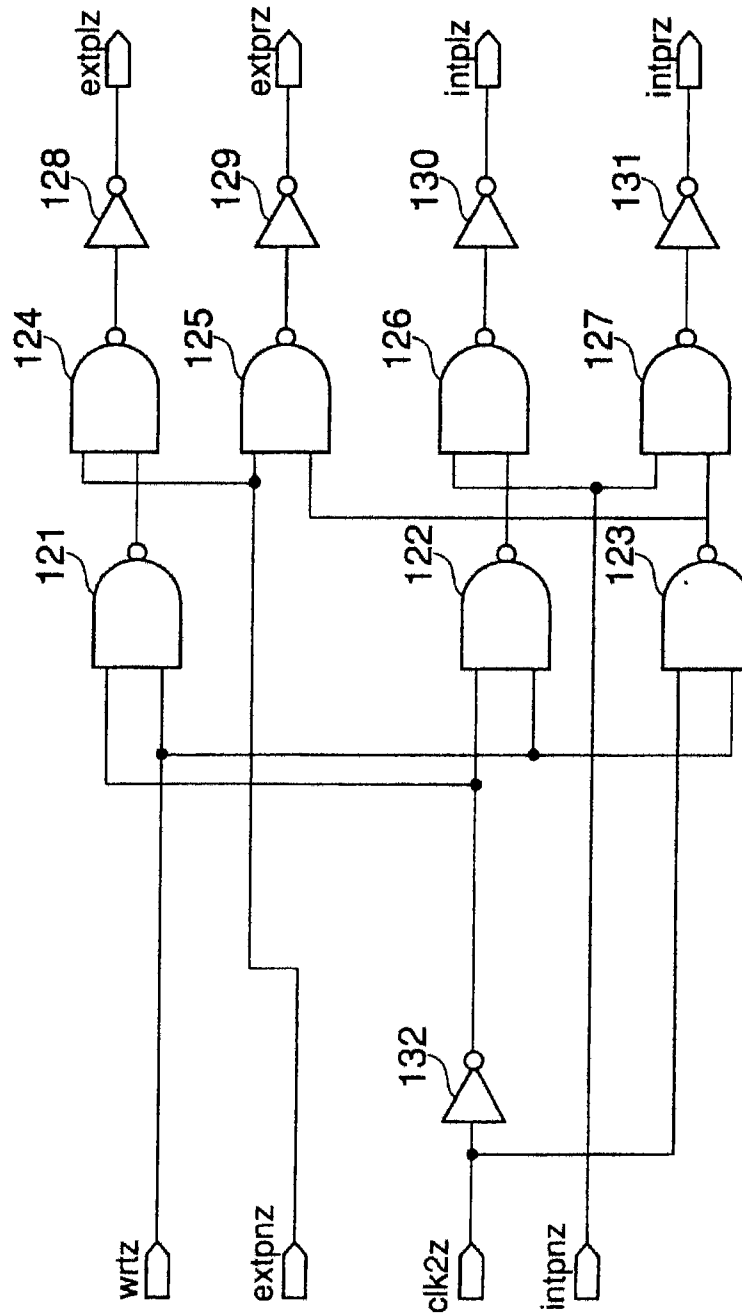
Sep. 18, 2001

Sheet 6 of 25

US 6,292,428 B1

FIG. 6

20





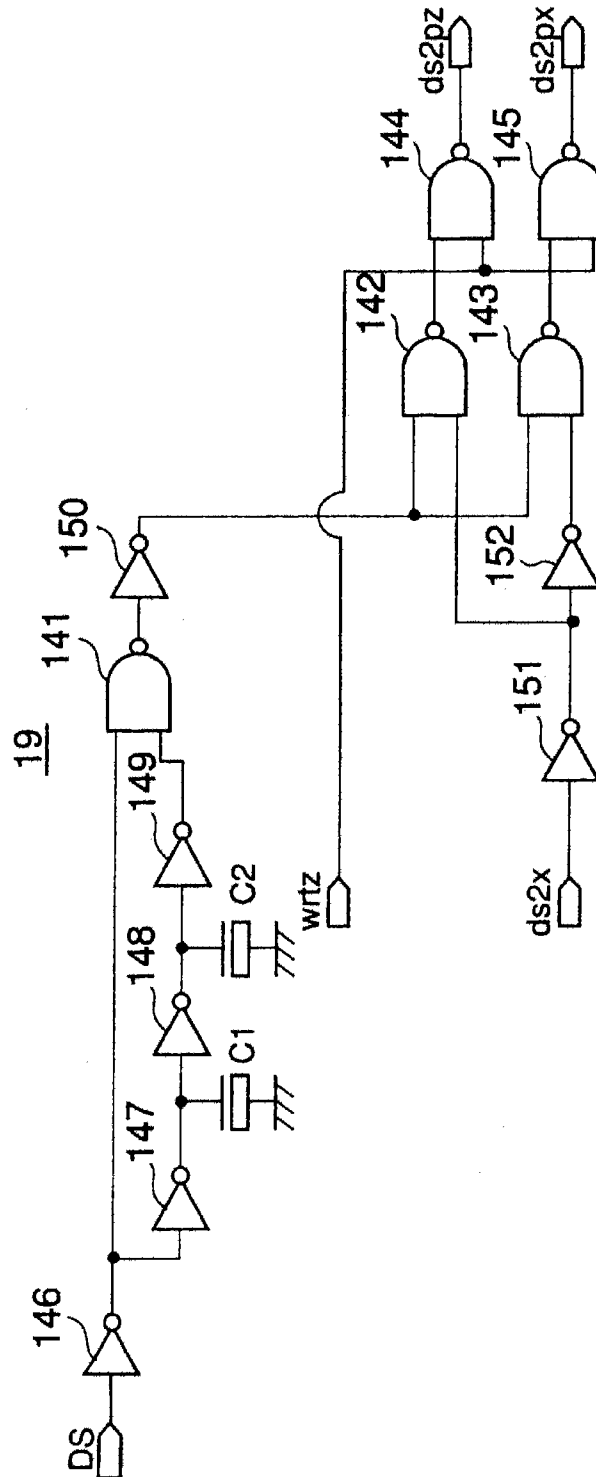
U.S. Patent

Sep. 18, 2001

Sheet 7 of 25

US 6,292,428 B1

FIG. 7



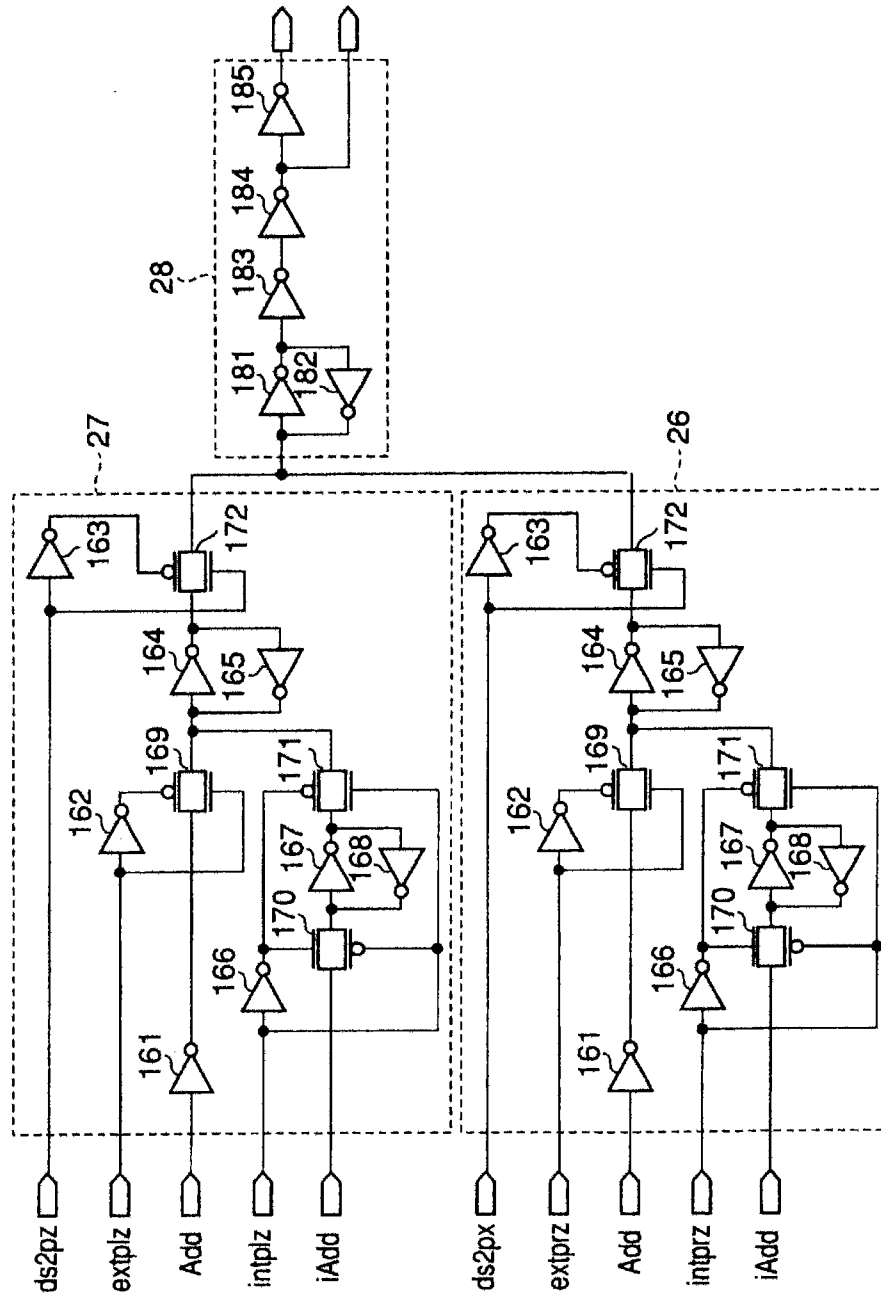
U.S. Patent

Sep. 18, 2001

Sheet 8 of 25

US 6,292,428 B1

FIG. 8



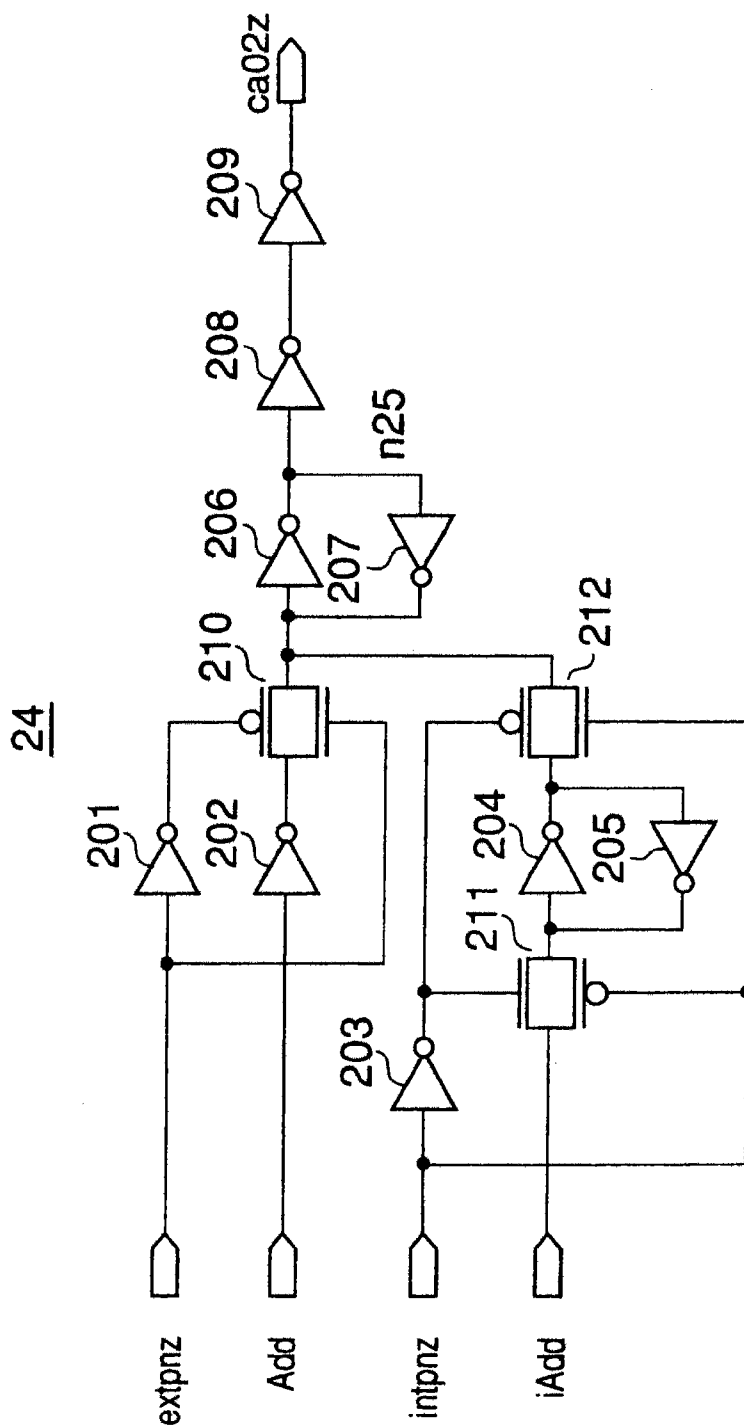
U.S. Patent

Sep. 18, 2001

Sheet 9 of 25

US 6,292,428 B1

FIG. 9



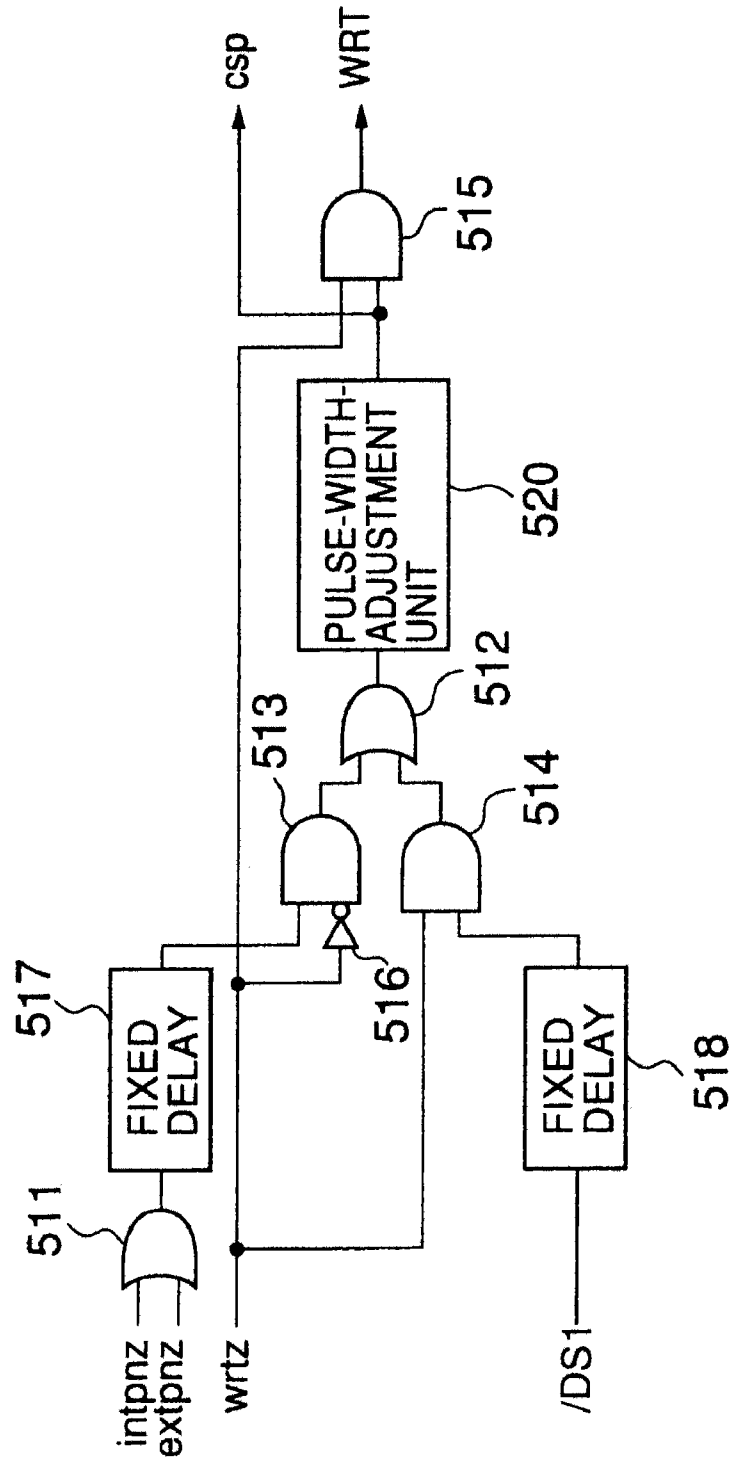
U.S. Patent

Sep. 18, 2001

Sheet 10 of 25

US 6,292,428 B1

FIG. 10

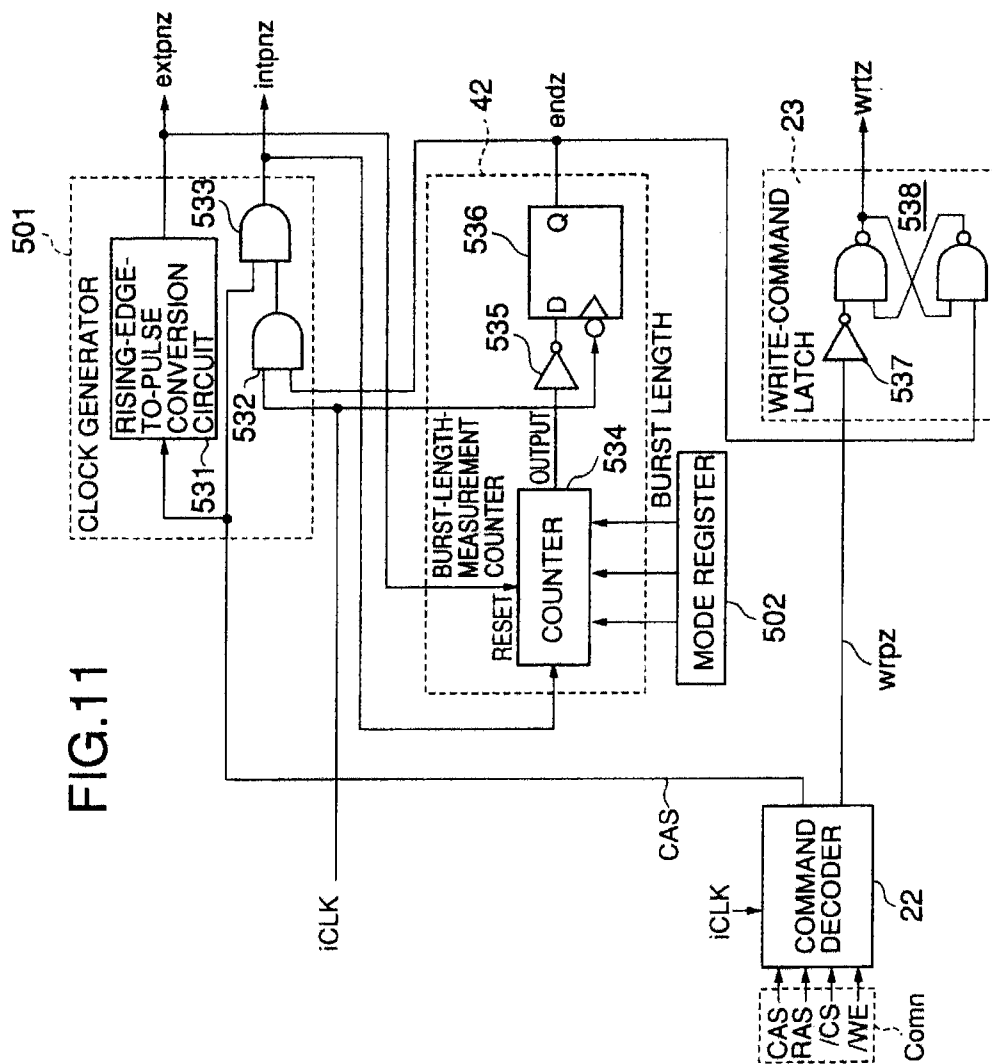


U.S. Patent

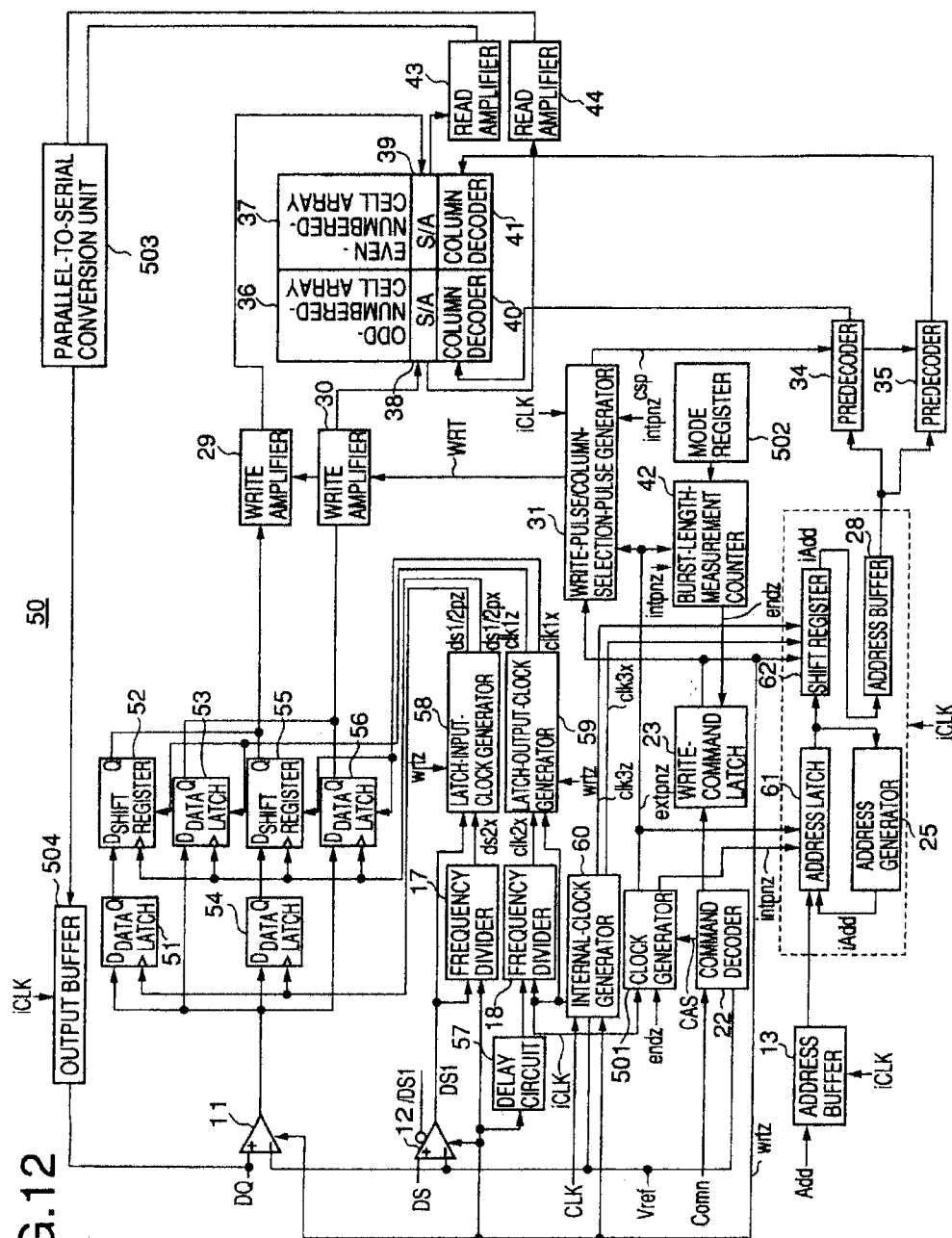
Sep. 18, 2001

Sheet 11 of 25

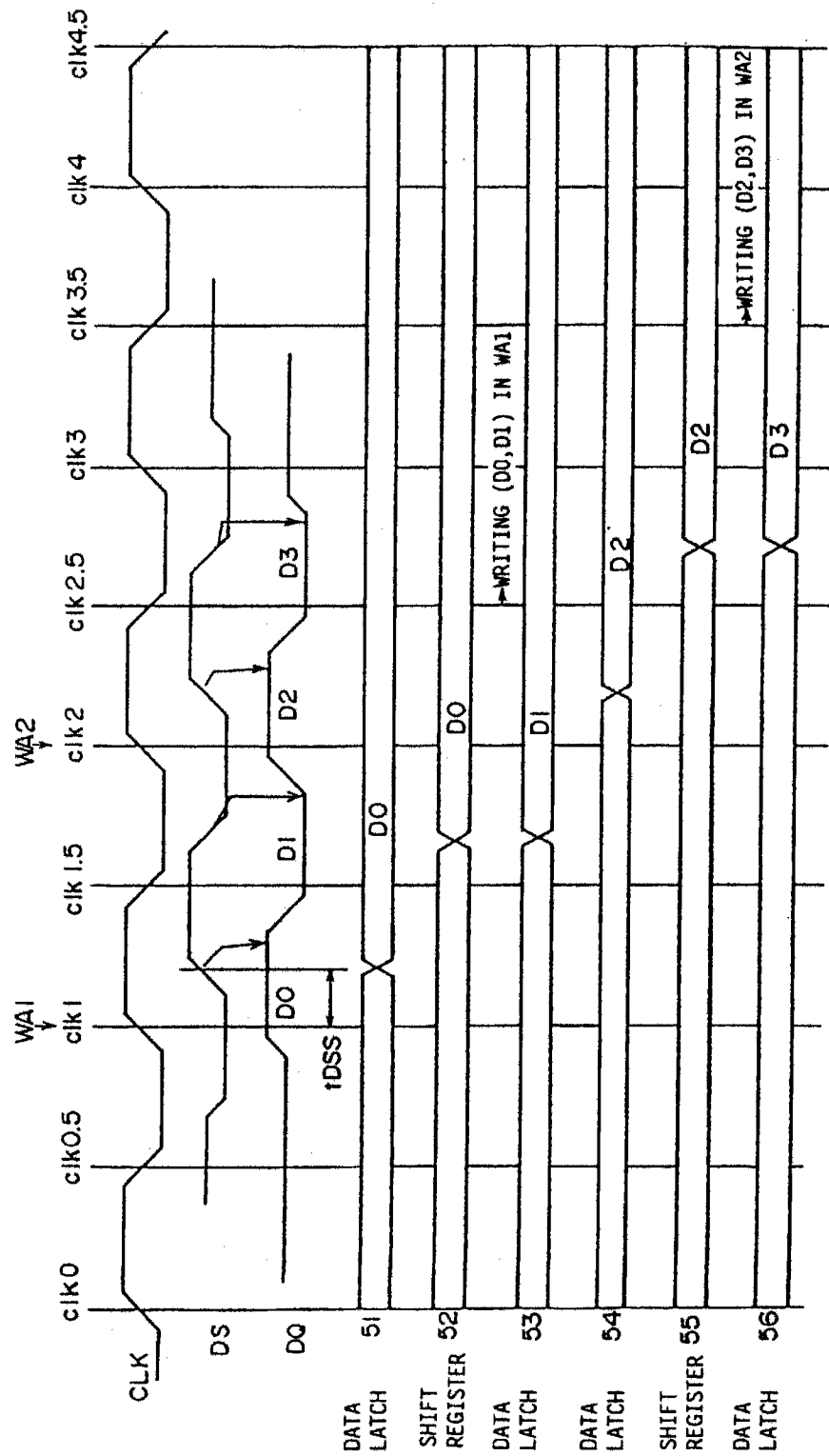
US 6,292,428 B1



**FIG. 12**



**FIG. 13**



U.S. Patent

Sep. 18, 2001

Sheet 14 of 25

US 6,292,428 B1

FIG. 14

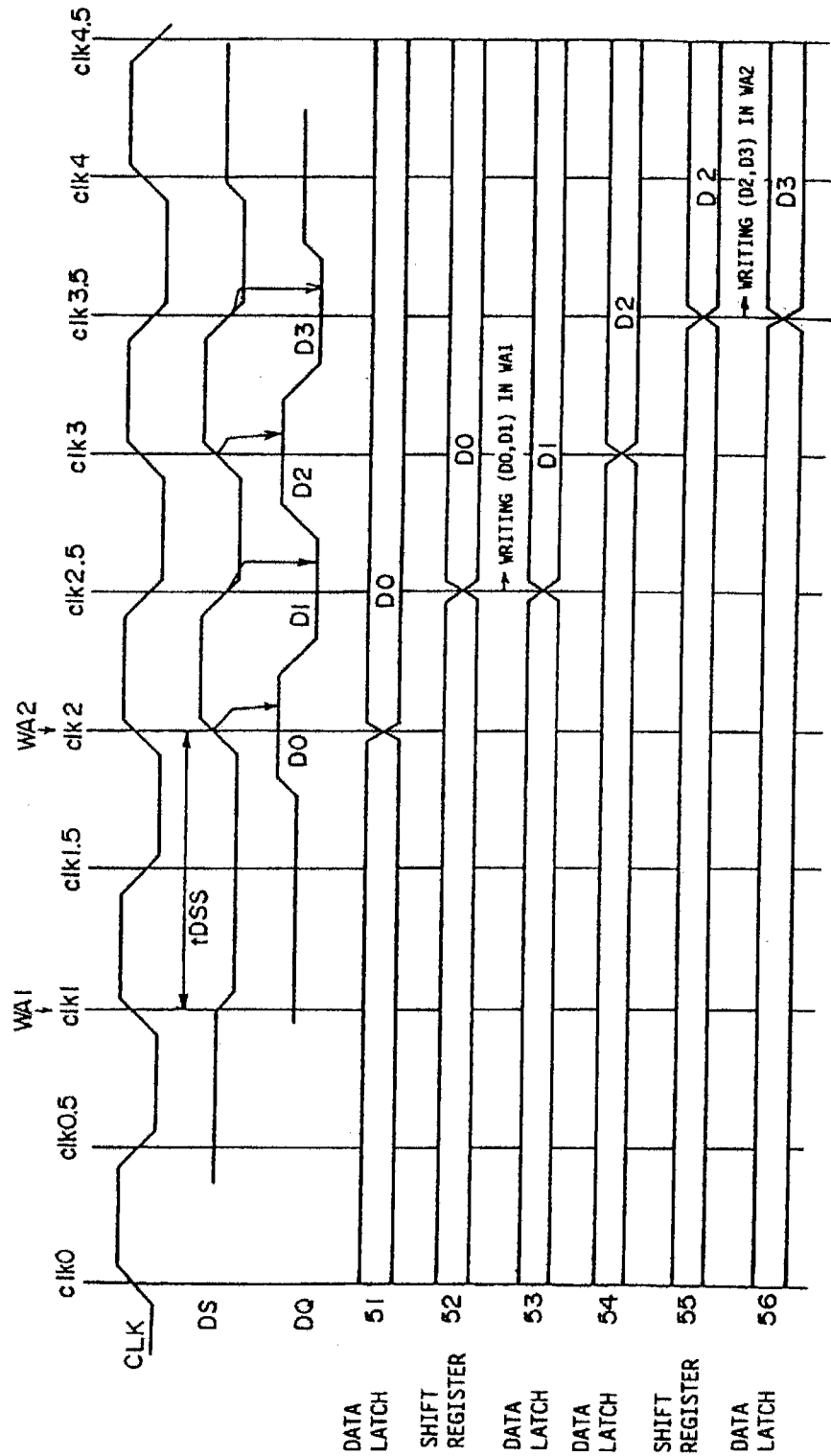
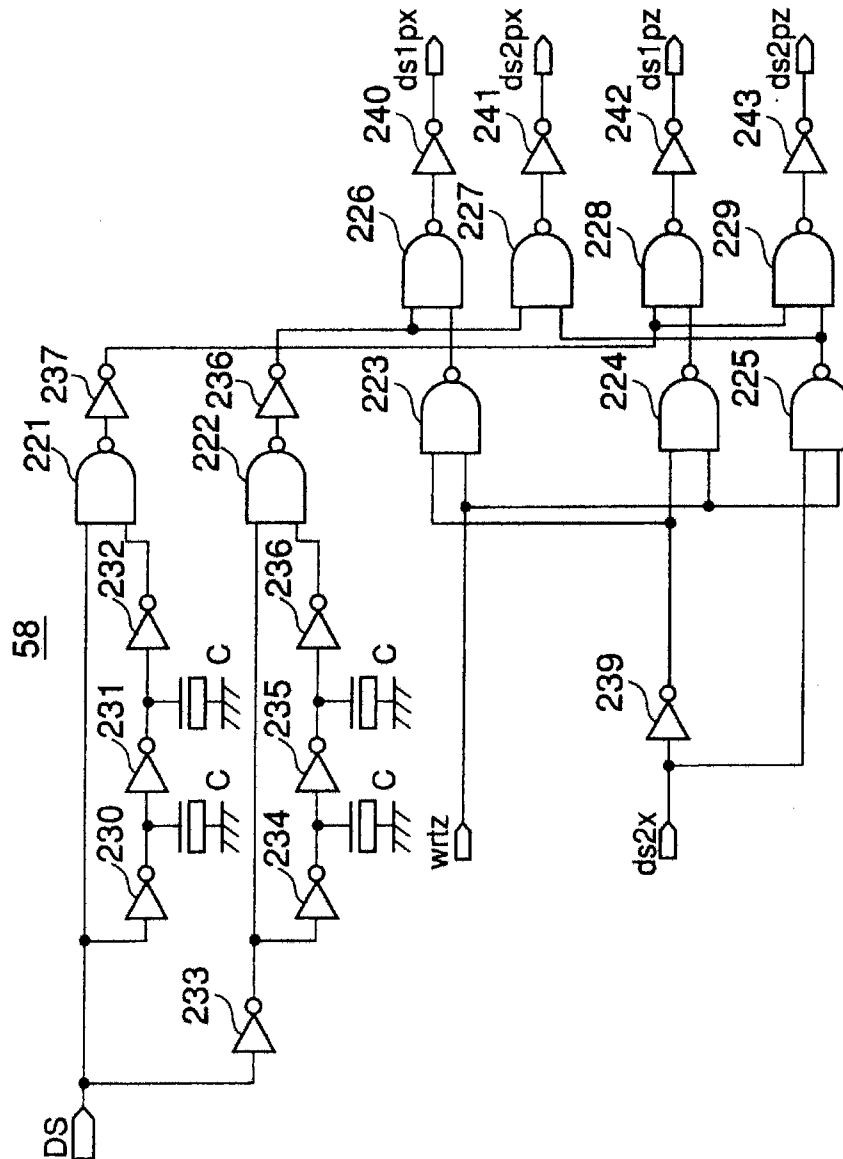




FIG. 15



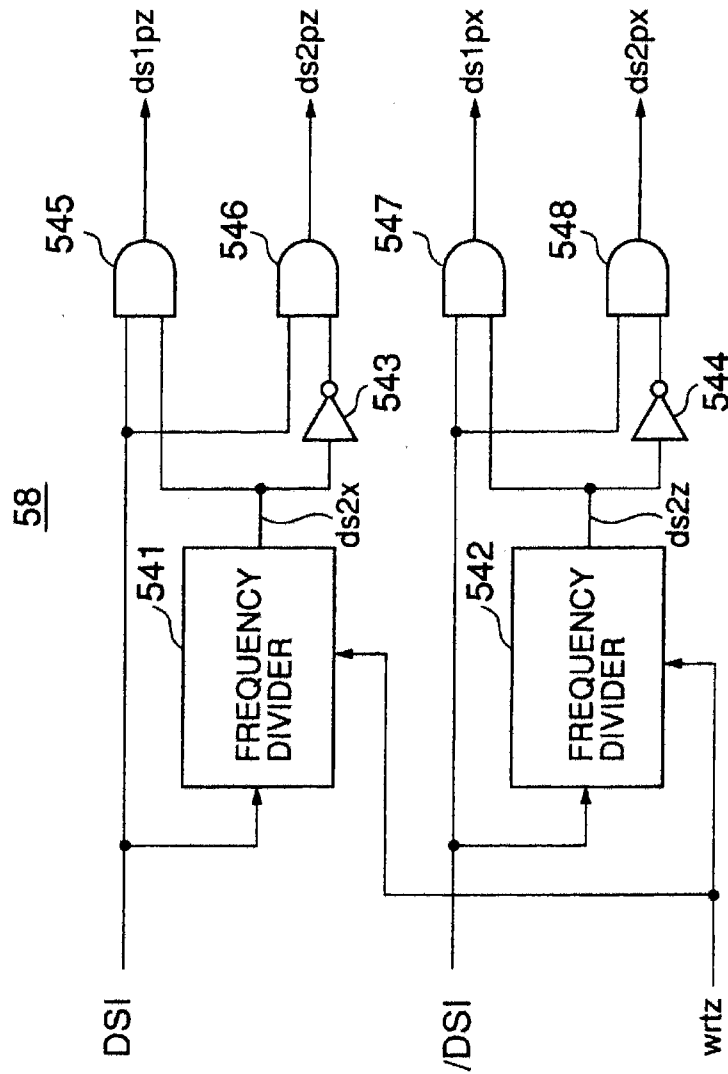
U.S. Patent

Sep. 18, 2001

Sheet 16 of 25

US 6,292,428 B1

FIG. 16



U.S. Patent

Sep. 18, 2001

Sheet 17 of 25

US 6,292,428 B1

FIG. 17

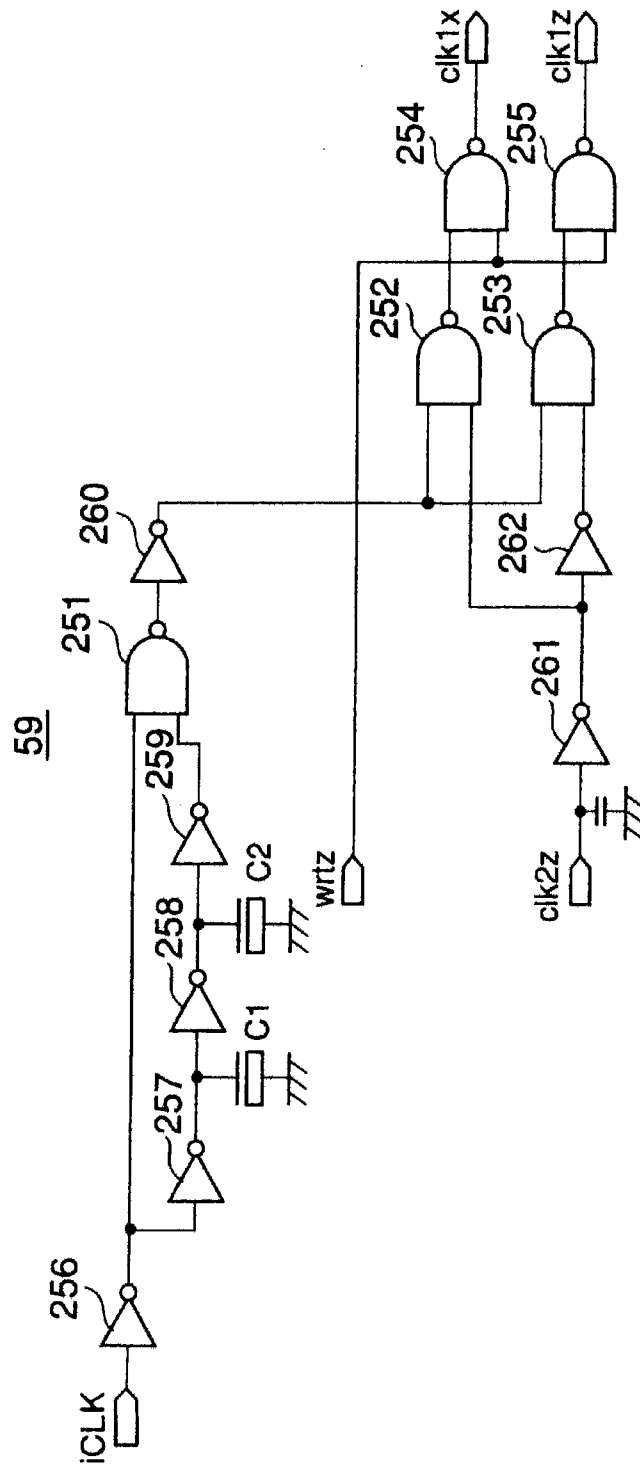
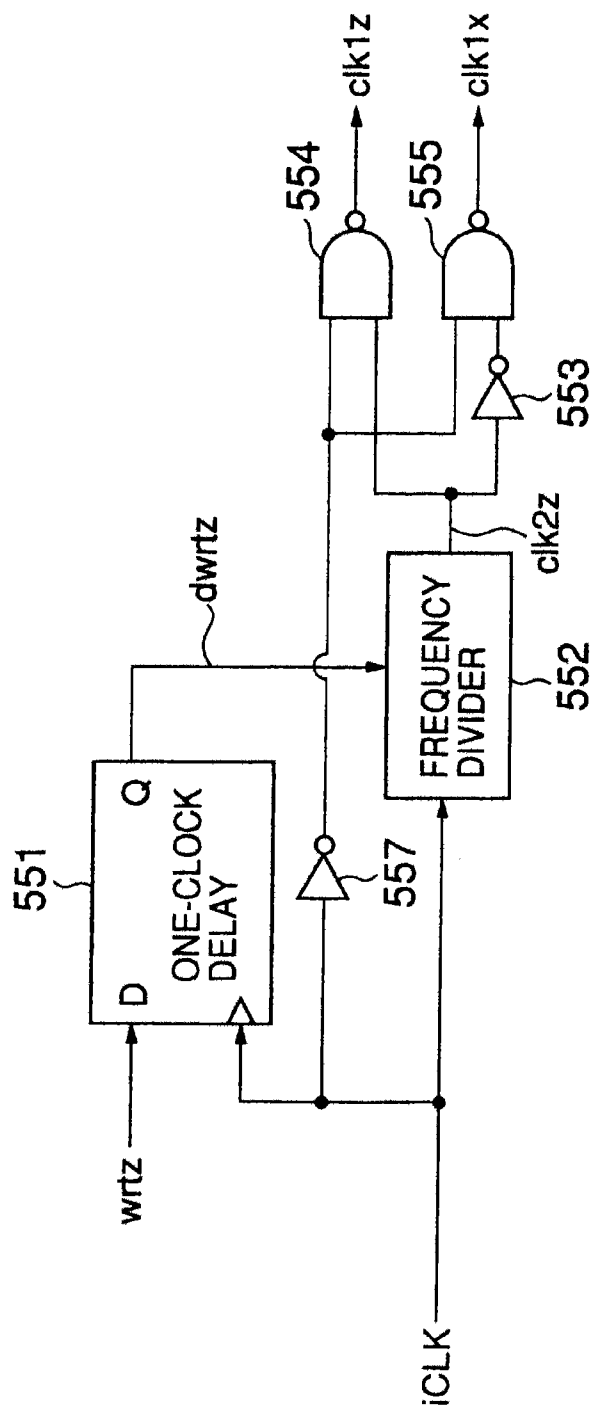


FIG. 18

59



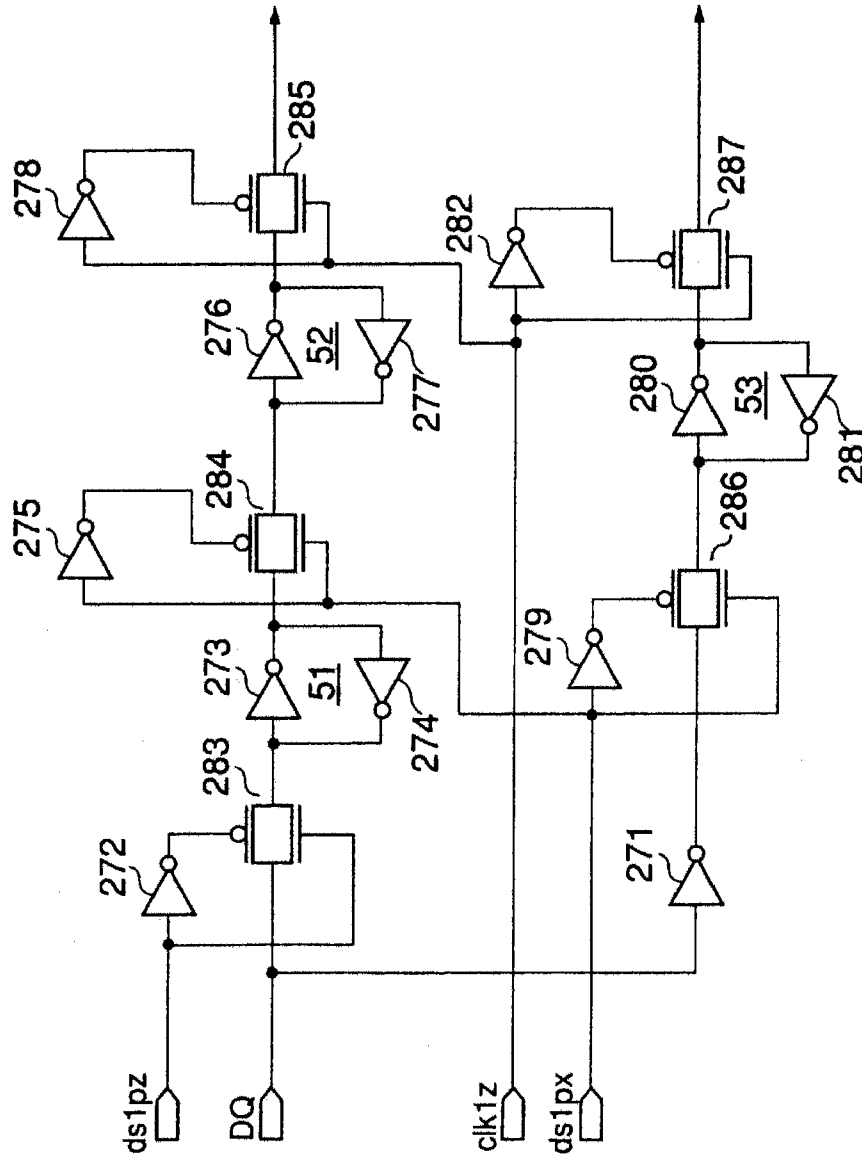
U.S. Patent

Sep. 18, 2001

Sheet 19 of 25

US 6,292,428 B1

FIG. 19



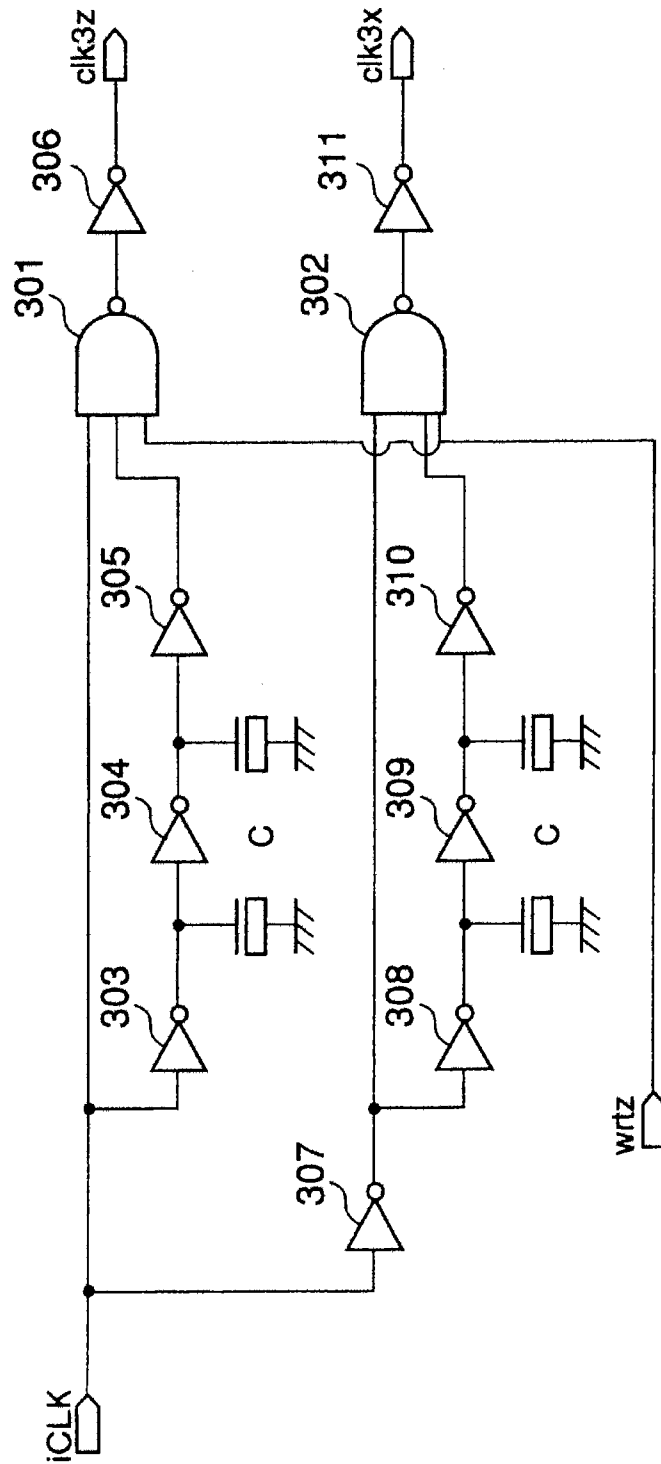
U.S. Patent

Sep. 18, 2001

Sheet 20 of 25

US 6,292,428 B1

FIG. 20



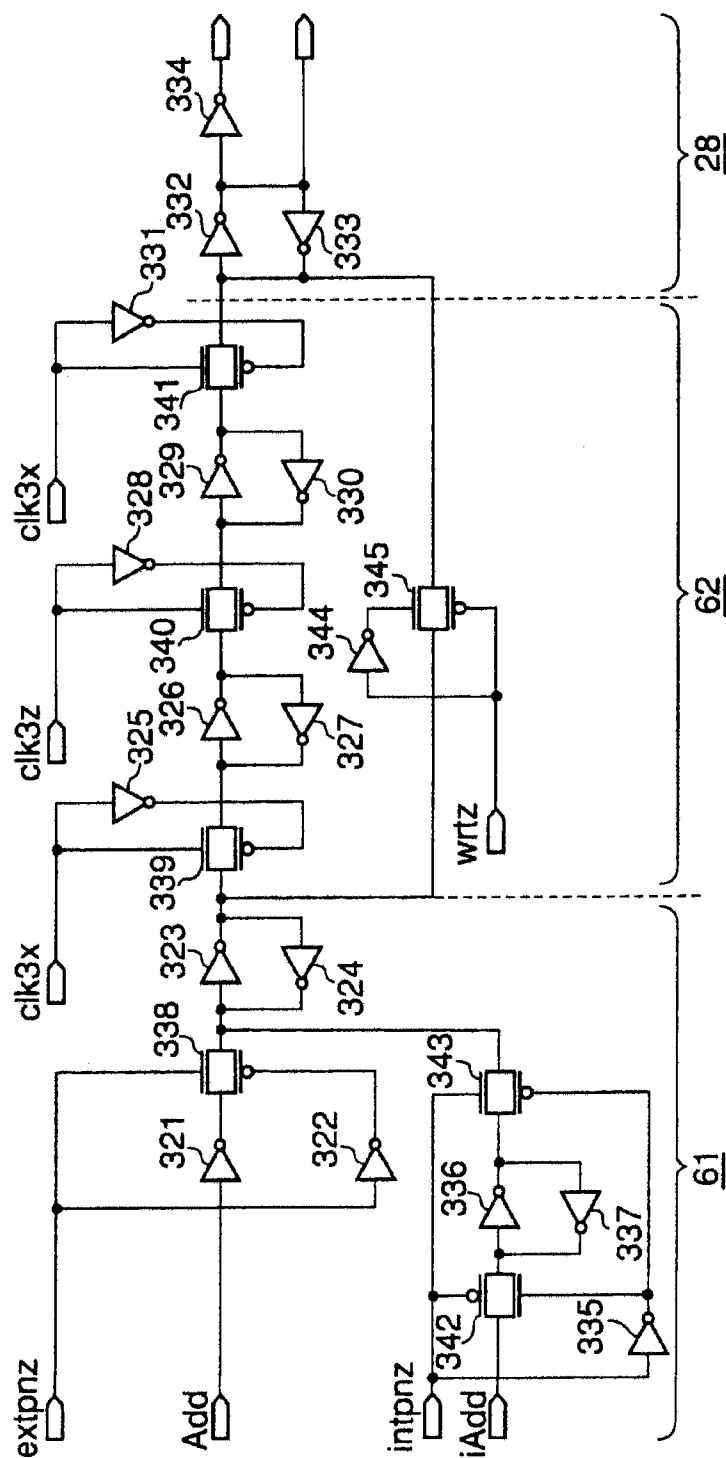
U.S. Patent

Sep. 18, 2001

Sheet 21 of 25

US 6,292,428 B1

FIG. 21



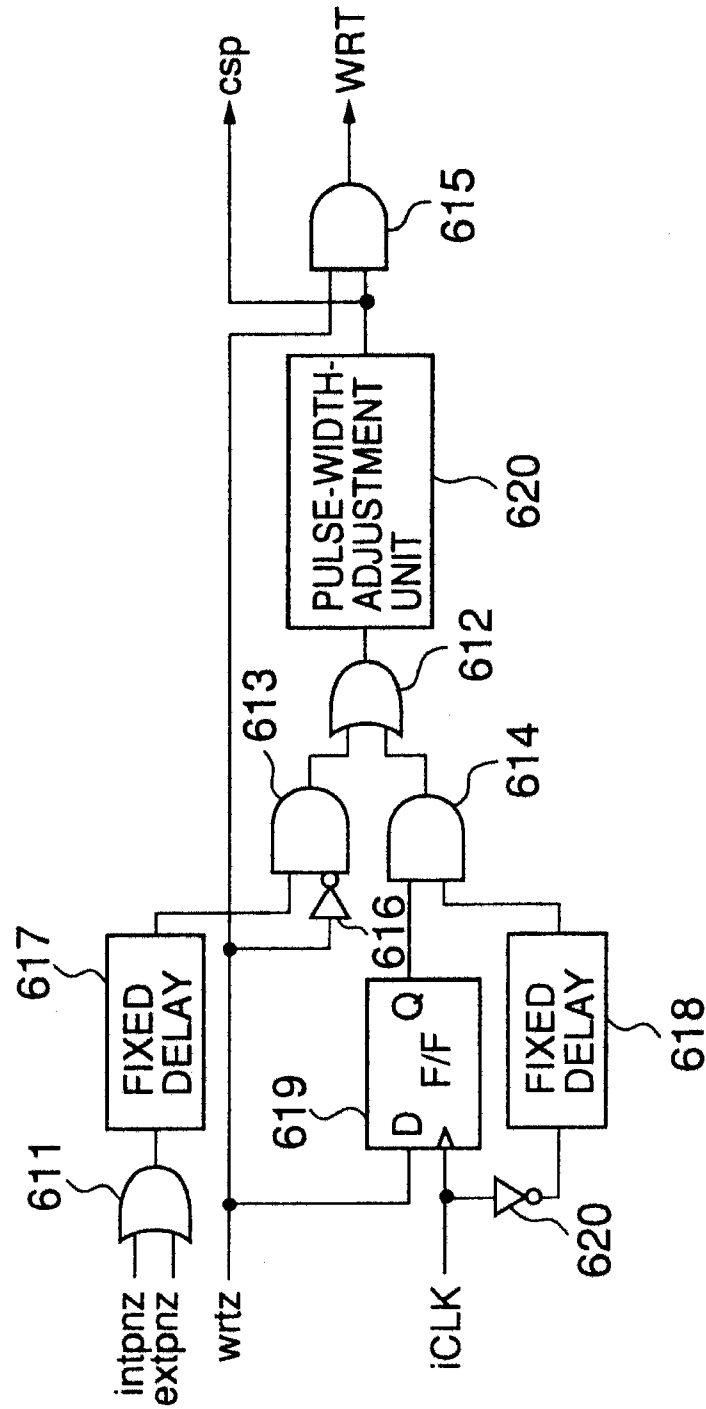
U.S. Patent

Sep. 18, 2001

Sheet 22 of 25

US 6,292,428 B1

FIG. 22





U.S. Patent

Sep. 18, 2001

Sheet 23 of 25

US 6,292,428 B1

FIG. 23

